Integrated CMOS Tri-Gate Transistors: Paving the Way to Future Technology Generations

Robert S. Chau, Intel Senior Fellow

Table of Contents

(Click on page number to jump to sections)

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Overview: Continuing Transistor Performance and Scaling Trends While Controlling Parasitic Leakages

The semiconductor industry continues to push technological innovation to keep pace with Moore's Law, shrinking transistors so that ever more can be packed on a chip. However, at future technology nodes, the ability to shrink transistors becomes more and more problematic, in part due to worsening short channel effects and an increase in parasitic leakages with scaling of the gate-length dimension. Both transistor off-state leakage (which increases with reducing gate length dimension) and gate oxide leakage (which increases with decreasing gate dielectric thickness) are contributing to the increase in power dissipation with scaling.

To address the transistor off-state leakage issue, in 2002 Intel developed the world's first CMOS tri-gate transistor,[1] which employs a novel three-dimensional gate design that improves the drive current while reducing the leakage current when the transistor is in the off state. Since then, Intel has further improved the performance and energy efficiency of the transistor by integrating the tri-gate design with other silicon process technology and material innovations, including strained silicon, high-k gate dielectrics, metal gate electrodes, and epitaxially raised source/drain. The result is a non-planar transistor that can provide 30 percent higher NMOS drive current and 60 percent higher PMOS drive current than the optimized, state-of-the-art 65nm-node planar transistors at the same off-state leakage.[2] This result shows that the benefits of the various silicon innovations are indeed additive and can be combined to extend and continue the CMOS scaling and performance trends.

Elevating CMOS Transistor Design to Three Dimensions

Since their inception in the late 1950s, planar transistors have acted as the basic building block of microprocessors. The scaling of planar transistors requires the scaling of gate oxides and source/drain junctions. However, as these transistor elements become harder to scale, so does the transistor gate length. The scaling of planar transistors is getting more difficult due to the worsening electrostatics and short-channel performance with reducing gate-length dimension.

A new transistor architecture that can significantly improve the electrostatics and short-channel performance is the tri-gate transistor, as shown in **Figure 1**. This transistor, which can be fabricated either on the SOI substrate or standard bulk-silicon substrate, has a gate electrode on the top and two gate electrodes on the sides of the silicon body. The top-gate transistor has physical gate length L_G and physical gate width W_{Si}, while the side-gate transistor has physical gate length L_G and physical gate width H_{Si}, as shown in **Figure 1**.

In general, the electrostatics, hence the short channel performance, of the tri-gate transistor is a function of the ratio of the effective L_G to the effective W_{Si}. The scaling of W_{Si} provides an additional knob to improve transistor electrostatics with L_G scaling, in addition to gate oxide and source/drain junction scalings. The total raw drive current of the transistor is a function of the sum of the drive currents contributed by the top-gate transistor and the two side-gate transistors, which in turn is a function of the sum of $2*H_{Si}$ and W_{Si}. Thus the taller the transistor, the higher the total raw drive current.

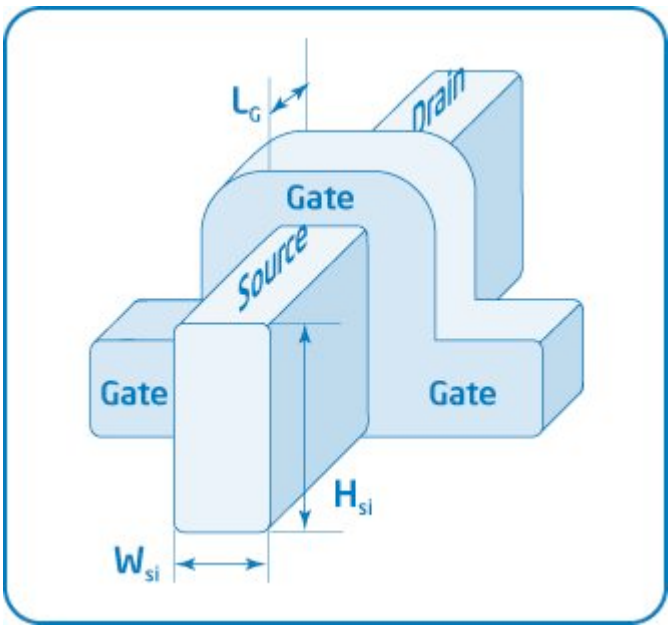

Figure 1. In the Intel® tri-gate transistor, gates surround the silicon channel on three of four sides.

Enhancing Design Through Innovative Integration

For faster and cooler operation of the non-planar transistors, Intel further enhanced the tri-gate design by integrating it with several advanced semiconductor technologies:

Strain engineering: Intel has been using strain engineering in its 90nm and 65nm process planar NMOS and PMOS transistors to improve their performance and is applying the technique to the non-planar tri-gate architecture. Strain engineering improves both the electron mobility and hole mobility of the tri-gate CMOS transistors and enhances CMOS transistor performance.

High-k/metal gate stack: The tri-gate CMOS transistors use a high-k (dielectric constant) material to replace the transistor's traditional silicon dioxide dielectric, and also replace the conventional polysilicon gate electrode with metal gate electrodes with workfunction close to the midgap. The use of the high-k/metal-gate stack reduces the gate oxide leakage compared to the standard SiO2/polysilicon gate stack. The use of metal electrodes eliminates polysilicon depletion and enhances transistor performance. In addition, the use of metal electrodes with close-to-midgap workfunctions also allows the reduction of substrate doping concentrations, thus enhancing transistor mobilities and hence overall transistor performance.

Dual epitaxial raised source/drain structure: The integrated CMOS tri-gate transistor uses a unique raised source/drain structure built up through epitaxial deposition of silicon for the NMOS transistor and SiGe for the PMOS transistor. The source and drain regions are raised with respect to the plane of the gate oxide-silicon substrate interface to reduce parasitic resistance, which improves device performance.

Intel has manufactured prototypes of the integrated tri-gate CMOS transistors on SOI as well as bulk-silicon substrates. The tri-gate transistor on bulk silicon and on SOI demonstrates equivalent scaling and short-channel performance and transistor drive performance.

Improving Performance with Integrated Tri-Gate Transistors

In benchmark testing, Intel demonstrated that integrated tri-gate NMOS and PMOS transistors showed excellent control of short channel effects (SCE), leading to reduced parasitic leakages and decreased power consumption. The tri-gate transistors also demonstrated higher performance, in terms of drive current, compared to an optimized, state-of-the-art planar 65nm-node transistor (see **Figure 2**). For a given transistor off-state leakage current (I_{OFF}), the integrated tri-gate NMOS transistor had 30 percent higher drive current (I_{DSAT}) than the planar transistor. This effect is even more pronounced for the integrated tri-gate PMOS transistor, which produced 60 percent higher I_{DSAT} than the planar transistor at a given I_{OFF}.

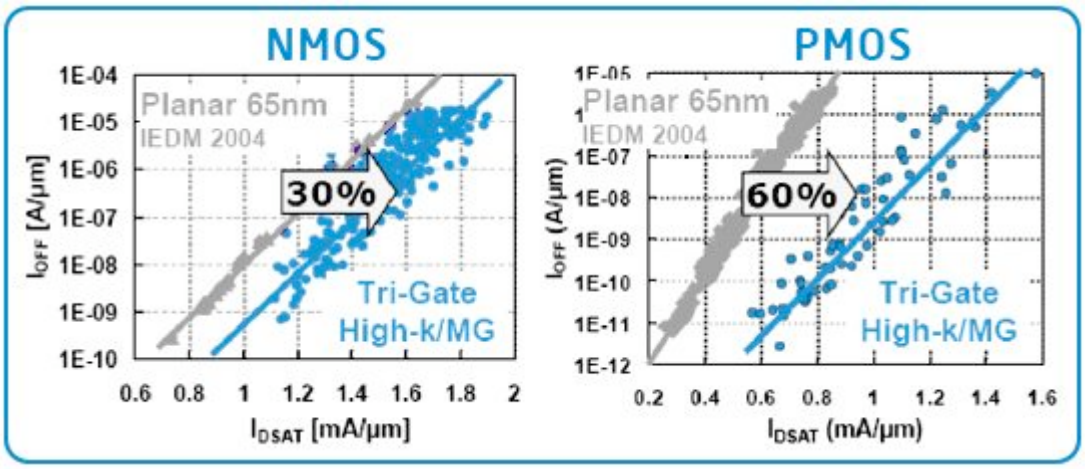

Figure 2. Integrated tri-gate NMOS and PMOS transistors demonstrate record drive current performance. The drive current, I_{DSAT}, is normalized to the total device width, for example, $2*H_{Si} + W_{Si}$.

Intel has also produced functional tri-gate static RAM (SRAM) cells (see Figure 3) with a cell read current 1.5 times higher than that of standard planar SRAM cells. By building upward, as shown in **Figure 4**, the tri-gate architecture provides more device width for a given cell footprint compared to the standard planar transistor—thus providing a higher read current because total current is a direct function of the total device width.

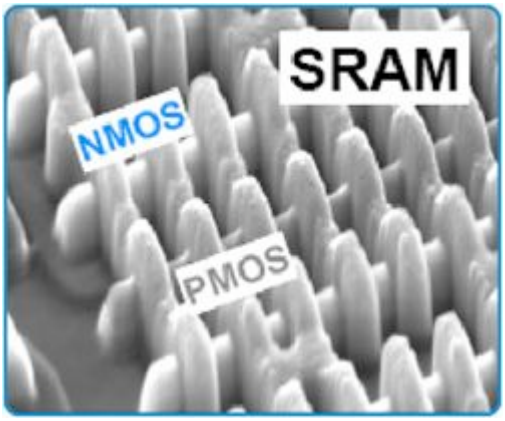

Figure 3. Close-up of tri-gate SRAM cells.

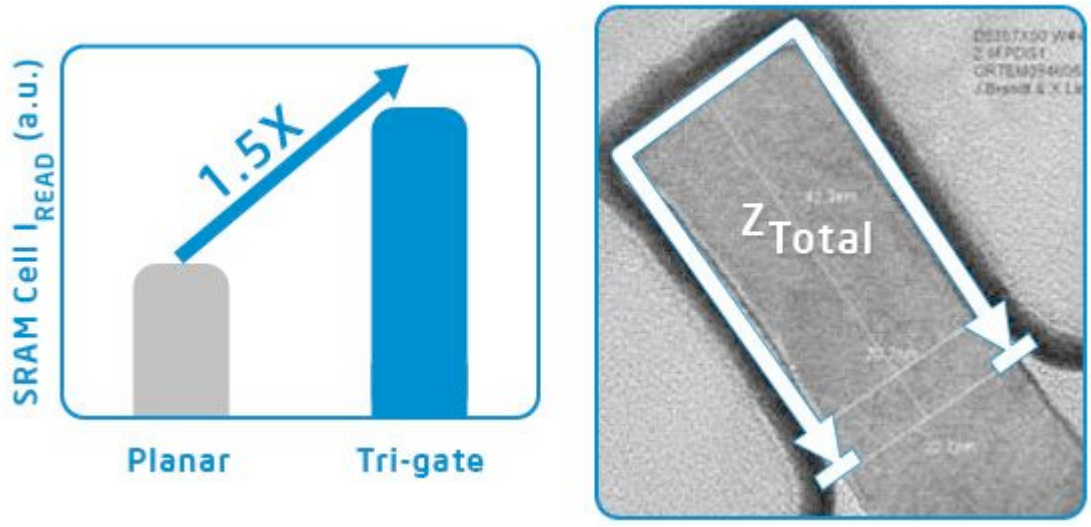

Figure 4. A tri-gate SRAM cell shows 1.5x higher cell read current compared to the standard planar SRAM cell of equivalent cell size due to higher total device width $Z_{total}=2*H_{Si}+W_{Si}$.

Summary

As transistors get smaller, parasitic leakage currents and power dissipation become significant issues. By integrating the novel three-dimensional design of the tri-gate transistor with advanced semiconductor technology such as strain engineering and high-k/metal gate stack, Intel has developed an innovative approach toward addressing the current leakage problem while continuing to improve device performance.

The integrated CMOS tri-gate transistors will play a critical role in Intel's energy-efficient performance philosophy because they have a lower leakage current and consume less power than planar transistors.

Because tri-gate transistors greatly improve performance and energy efficiency, they enable Intel to extend the scaling of silicon transistors. Intel expects that the tri-gate transistors could become the basic building block for microprocessors in future technology nodes. The technology can be integrated into an economical, high-volume manufacturing process, leading to high-performance and low-power products.

More Info

Learn more by visiting the following areas of the Intel Web site:

Silicon Technology and Manufacturing
Intel's Breakthrough in High-K Gate Dielectric Drives Moore's Law Well into the Future [PDF 102KB]
Energy-Efficient Performance
Moore's Law

Author Bio

Robert S. Chau, Intel Senior Fellow, Technology and Manufacturing Group Director, Transistor Research and Nanotechnology, Intel Corporation
Robert S. Chau is an Intel Senior Fellow and Director of Transistor Research and Nanotechnology in Intel's Technology and Manufacturing Group. Chau is responsible for directing research and development in advanced transistors and gate dielectrics, process modules and technologies, and silicon integrated processes for microprocessor applications. He is also responsible for leading research efforts in emerging nanotechnology for future nanoelectronics applications.

Chau joined Intel in 1989, and became an Intel Fellow in 2000 and an Intel Senior Fellow in 2005. During his career at Intel, he has developed nine generations of Intel gate dielectrics along with many transistor innovations and process modules and technologies used in various Intel manufacturing processes and microprocessor products. He also introduced many new process modules and novel nanotechnologies for Intel's future integrated circuit processes.

Chau received his bachelor's and master's degrees and Ph.D. in electrical engineering from The Ohio State University. He holds more than 90 issued United States patents, and has received six Intel Achievement Awards and 13 Intel Logic Technology Development Division Recognition Awards. He was recognized by *IndustryWeek* in 2003 as one of the 16 "R&D Stars" in the United States who "continue to push the boundaries of technical and scientific achievement." Chau is an IEEE Fellow.

Notes

[1] R. Chau, B. Doyle, J. Kavalieros, D. Barlage, A. Murthy, M. Doczy, R. Arghavani, and S. Datta. "Advanced Depleted-Substrate Transistors: Single-Gate, Double-Gate, and Tri-Gate," Extended Abstracts of the International Conference on Solid-State Devices and Materials (SSDM), Nagoya, Japan, 2002, pp. 68-69.
[2] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau. "Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates, and Strain Engineering," VLSI Technology Digest of Technical Papers, June 2006, pp. 62-63.

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